Data Processing in Digital Systems

Abstract of the Disclosure

A structure comprising an FPGA (Field-Programmable Gate Array) for relieving bottlenecks, and a method for operating the structure. The FPGA comprises multiple FPGA elements each of which includes a CLB (Configurable Logic Block), an instruction queue, and a data buffer. One functional block after another (separate from one another) can be formed in the FPGA via a first local IO (Input/Output) circuit and moved to a second local IO circuit. Within each functional block, a mapped logic location function calculates the direction, distance, and the time for the step from the current location of the functional block stored in a mapped location register, and the destination stored in a mapped destination register, and the time allowed for the movement, and stores the direction and distance of the step in the mapped movement register. Then, the functional block moves according the direction and distance stored in the mapped movement register.